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(54) D TYPE FLIP-FLOP

(57) Abstract:

PROBLEM TO BE SOLVED: To shorten a hold time, speed up operation, and lower power consumption by connecting two stages of master-side latches, which function to hold only a low level, in series.

SOLUTION: The master-side latches A and B both hold only the low level. Then the output node 12 of the master-side latch A is connected to the input node 14 of a slave-side latch C and also connected to the input node 13 of the master-side latch B. Consequently, a high level and the low level are both held at the output node 12' of the master-side latch B. Therefore, even if input data at an input terminal D varies from the high level to the low level after a clock signal CLK varies to the high level, the high-level signal held at the output node 12' never disappears and write to the slave-side latch C which is carried out through a transistor 6 as a 2nd data transmitting means is never interrupted right after the clock signal CLK goes up to the high level.